PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/768, 23/532

A1

(11) International Publication Number: WO 97/18585

(43) International Publication Date: 22 May 1997 (22.05.97)

(21) International Application Number: PCT/US96/14340

(22) International Filing Date: 5 September 1996 (05.09.96)

(30) Priority Data:
08/559,054 16 November 1995 (16.11.95) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: NGO, Minh, Van; 5147 Capitola Way, Union City, CA 94587 (US). CHAN, Darin, A.; 2054 Anthony Drive, Campbell, CA 95008 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

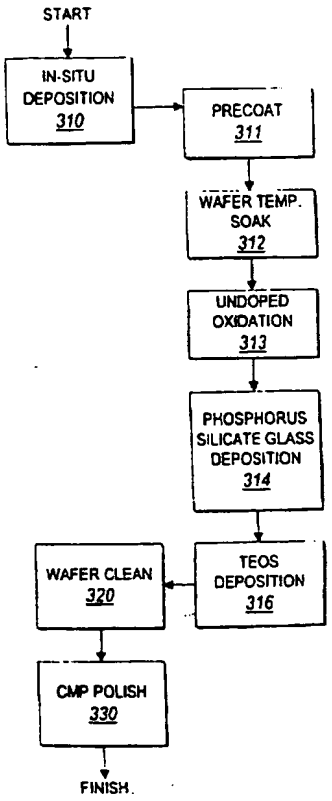
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: TRI-LAYER PRE-METAL INTERLAYER DIELECTRIC COMPATIBLE WITH ADVANCED CMOS TECHNOLOGIES

(57) Abstract

A method of depositing a premetal dielectric layer (110) on a semiconductor substrate (102) involves depositing of a triple premetal dielectric layer (110) in in-situ deposition in a single fabrication tool with each subsequent layer being deposited after a previous layer with no intervening handling step. Thus, no intervening cleaning steps or other intermediate steps are performed; the substrate is then cleaned and chemical mechanical polished.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

TRI-LAYER PRE-METAL INTERLAYER DIELECTRIC COMPATIBLE WITH ADVANCED CMOS TECHNOLOGIES

Minh Van Ngo
Darin A. Chan

Field of the Invention

This invention relates to the field of integrated circuit fabrication methods and, more specifically, to integrated circuit fabrication methods for depositing a premetal interlayer dielectric.

Background of the Invention

Fabrication of semiconductor devices involves the application of numerous fabrication steps. Each of the fabrication steps extracts a cost in terms of time and handling. Generally, a process that involves fewer handling steps generally produces electronic devices at a much lower cost than a process that produces the same quality devices using more handling steps.

Each structure in a semiconductor device is produced by a series of fabrication steps. One such structure is a premetal interlayer dielectric deposition. A premetal interlayer dielectric is a dielectric layer that is typically formed between polysilicon and a metal interconnect layer so that all of the devices underlying the metal interconnect layer are electrically isolated.

A conventional process for forming a premetal interlayer dielectric on a semiconductor wafer requires many fabrication steps. These steps include a low temperature oxidation deposition step to form a barrier layer and cleaning operation prior to low temperature oxidation. The cleaning operation is performed in a different tool (a sink) than the low temperature oxidation tool (a furnace). Following the low temperature oxidation, the wafer is again removed from the furnace for cleaning. After cleaning, a boron-phosphorous TEOS deposition is performed in a PECVD reactor to form a second layer of oxide film. Densification of the two-layer film is achieved by thermal cycling in a furnace. Densification reflows the oxide at elevated temperatures and results in some planarization of the surface of the semiconductor wafer. Following densification, the wafer is again cleaned. The wafer is then inspected for BPO_4 crystal defects that may occur in densification. The wafer is then etched back in a reactor to give the final form of the premetal interlayer dielectric. The many steps used in this process result in an increase in fabrication costs.

What is needed is a method for depositing a premetal interlayer dielectric that greatly reduces handling steps and thus reduces fabrication costs.

Summary of the Invention

In accordance with the present invention, a method of depositing a premetal dielectric layer involves deposition of a triple premetal dielectric layer in in-situ deposition in a single fabrication tool with each subsequent layer being deposited after a previous layer with no intervening handling step. Thus, no intervening cleaning steps or other intermediate steps are performed.

Several advantages are achieved by the described method. One advantage is that thermal cycling at high temperatures is not employed in the disclosed method. Many advanced technology devices utilize silicided gates and structures. A silicide film is not stable at high temperatures so that thermal cycling during densification damages the silicide, causing agglomeration of atoms within the silicide and raising the resistivity in the circuit. Low resistivity is a desired trait of silicides. In the disclosed method, the temperature does not exceed 800 degrees Celsius so that titanium silicide structures are not damaged.

Another advantage of the disclosed method is that the defect rate of fabricated devices is very low due to the reduction in handling. A further advantage of the method that results from the reduced handling is a substantially reduced manufacturing cost.

Brief Description of the Drawings

The features of the invention believed to be novel are specifically set forth in the appended claims. However, the invention itself, both as to its structure and method of operation, may best be understood by referring to the following description and accompanying drawings.

Figure 1 is a cross-sectional view of an integrated circuit wafer showing an example of a trilayer premetal interlayer dielectric.

Figure 2 is a pictorial representation of a PECVD reactor for depositing a tri-layer premetal interlayer dielectric in accordance with one embodiment of the present invention.

Figure 3 is a flow chart which illustrates steps of a method for depositing a trilayer premetal interlayer dielectric in accordance with the present invention.

Detailed Description

Referring to **Figure 1**, a cross-sectional view of an integrated circuit **100** shows an example of a trilayer premetal interlayer dielectric deposition. The integrated circuit **100** includes a silicon substrate **102**. A field oxide region **104** is formed on one side of the substrate **102** and is used to isolate devices within the substrate **102**. A plurality of polysilicon gates **106** are formed overlying the substrate **102**. The polysilicon gates **102** have oxide spacers **108** for implantation of structures such as lightly-doped drain (LDD) structures. A tri-layer premetal dielectric **110** overlies the surface of the substrate **102**. The three layers of the tri-layer

premetal dielectric 110 include an undoped liner/barrier layer 112, a doped gettering layer 114 and an undoped TEOS layer 116. A solid line 120 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after deposition of the tri-layer but before any etching or polishing. A dotted line 122 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after chemical mechanical polishing.

The doped gettering layer 114 has a thickness of approximately 3000 angstroms. The doped gettering layer 114 is employed to attract and hold electrons and holes and to prevent the electrons and holes from migrating and affecting transistor performance. Otherwise, these electrons and holes may act to create leakage currents, shift threshold voltages and the like. The undoped liner/barrier layer 112 is used to chemically isolate the doped gettering layer 114 from the polysilicon gates 102. Polysilicon gates 102 often are P+type doped, for example with boron. Phosphorus in the doped gettering layer 114 would act as an antidopant to the boron of the polysilicon gates 102 so that the undoped liner/barrier layer 112 is provided to prevent counter doping of the boron by the phosphorus. The undoped liner/barrier layer 112 has a thickness of approximately 500 angstroms.

The undoped TEOS layer 116 is utilized to fill any voids in the surface of the doped gettering layer 114. The undoped TEOS layer 116 fills voids caused by structures such as the polysilicon gates 102 and the field oxide region 104. The undoped TEOS layer 116 also adds thickness to the surface of the integrated circuit so that all structures, even prominant structures overlying both the field oxide region 104 and the polysilicon gate 102. The undoped TEOS layer 116 has a

thickness of approximately 10200 angstroms. The total thickness of the trilayer premetal dielectric **110** is approximately 13700 angstroms with a standard deviation of approximately 200 angstroms and a final thickness after polishing of about 4000 angstroms.

Referring to **Figure 2**, a PECVD reactor **200** for depositing a trilayer premetal dielectric is shown. In one embodiment of the method, a NOVELLUS CONCEPT 1 (TM) PECVD reactor **200** is used to the trilayer premetal dielectric in a silane (SiH_4)-based system. In this embodiment, reactant gases include silane (SiH_4), nitrous oxide (N_2O), molecular nitrogen (N_2), molecular oxygen (O_2) and TEOS.

The reactor **200** includes a chamber **202** holding a wafer **204**, an in-flow tube **206** for carrying reactant gases to the chamber **202**, a shower head **208** for applying the reactant gases to the chamber **202**. A heater block **210** heats the wafer **204** and also supports the wafer **204** during processing.

Referring to **Figure 3**, a flow chart illustrates steps of a method **300** for depositing a tri-layer premetal interlayer dielectric using in-situ deposition. The in-situ deposition method **300** includes a triple layer in-situ deposition step **310**. The triple layer in-situ deposition step **310** has five substeps including a precoat step **311**, a wafer temperature soak step **312**, an undoped oxidation step **313**, a phosphorus silicate glass deposition step **314** and a TEOS deposition step **316**. All of the substeps of the triple layer in-situ deposition step **310** take place in sequence in a single PECVD reactor so that no handling of semiconductor wafer occurs between any substeps. This reduction in handling results in a very low defect rate. Also, in the in-situ deposition

step 310, the semiconductor wafer is continually kept under vacuum. Because the wafer is kept under vacuum, cleaning between deposition of the constituent layers is not necessary.

Following the in-situ deposition step 310, the wafer is cleaned in wafer clean step 320 using standard wafer cleaning techniques that are well known in the art. Subsequent to the wafer clean step 320, chemical mechanical polish (CMP) step 330 polishes the wafer to attain a substantially flat surface by removing a portion of the TEOS layer 116. CMP step 330 employs a conventional chemical mechanical polish operation as is known in the art of semiconductor fabrication.

The precoat step 311 which occurs for a specified precoat time, as is known in the PECVD art, is employed for chamber seasoning. During the precoat step 311 operation, the wafer 204 is held outside the reactor 200 while reactant gases are applied to the chamber 202. The precoat step 311 coats the interior surfaces of the reactor 200. In precoat step 311, precoating is done for each of the undoped oxidation step 313, the phosphorus silicate glass deposition step 314 and the TEOS deposition step 316. Thus, while the wafer is outside the reactor 200, the reactant flows, power, pressure and temperature for each of the three deposition substeps is applied to the reactor 200 for a specified time. In one embodiment using the NOVELLUS CONCEPT 1 (TM) PECVD reactor, the precoat time for each deposition substep is 240 seconds. For example, the reactant flows, pressure, power and temperature utilized in undoped oxidation step 313 is first applied to the reactor 200 for 240 seconds. Then the reactant flows, pressure, power and temperature utilized in phosphorus silicate glass deposition step 314 is applied to the reactor 200 for 240 seconds. Finally,

the reactant flows, pressure, power and temperature utilized in TEOS deposition step 316 is applied to the reactor 200 for 240 seconds.

Following the precoat step 311, a wafer temperature soak operation as is known in the PECVD art, is applied in soak step 312. During the soak operation, a cold wafer 204 from outside the reactor 200 is placed into the chamber 202 and heated on the heaterblock 210 before reactant gases, power and pressure are applied to the chamber 202. A typical soak time using the NOVELLUS CONCEPT 1 (TM) PECVD reactor is approximately 60 seconds.

In the undoped oxidation step 313, the reactants including silane (SiH_4), nitrous oxide (N_2O) and molecular nitrogen (N_2) are applied by a flow into the chamber 202 at a selected pressure and RF power. In an embodiment of the present invention using the NOVELLUS CONCEPT 1 (TM) PECVD reactor to fabricate wafers, the silane (SiH_4) flow rate is approximately 200 sccm, although flow rates from 190 sccm to 210 sccm are suitable. The nitrous oxide (N_2O) flow rate is approximately 6000 sccm, although flow rates from 5700 sccm to 6300 sccm are suitable. A nitrogen (N_2) flow rate is approximately 3150 sccm although flow rates from 3000 sccm to 3300 sccm are suitable. High frequency power applied at approximately 600 watts and low frequency power at approximately 400 watts although wattages that vary from these values by plus or minus five percent are also suitable. Pressure is applied at about 2.2 torr although pressures from 2.0 torr to 2.4 torr are suitable. The deposition temperature is about 400 degrees Celsius. Deposition is applied for multiple seconds.

In phosphorus silicate glass deposition step 314, the reactants including silane (SiH_4), phosphene (PH_3),

nitrous oxide (N_2O) and molecular nitrogen (N_2) are applied by a flow into the chamber 202 at a selected pressure and RF power. In an embodiment of the present invention using the NOVELLUS CONCEPT 1 (TM) PECVD reactor to fabricate wafers, the silane (SiH_4) flow rate is approximately 200 sccm, although flow rates from 190 sccm to 210 sccm are suitable. The phosphene (PH_3) flow rate is approximately 320 sccm, although flow rates from 305 sccm to 335 sccm are suitable. The nitrous oxide (N_2O) flow rate is approximately 6000 sccm, although flow rates from 5700 sccm to 6300 sccm are suitable. A nitrogen (N_2) flow rate is approximately 2700 sccm, although flow rates from 2550 sccm to 2850 sccm are suitable. High frequency power applied at approximately 600 watts and low frequency power at approximately 400 watts although wattages that vary from these values by plus or minus five percent are also suitable. Pressure is applied at about 2.4 torr although pressures from 2.0 torr to 2.2 torr are suitable. The deposition temperature is about 400 degrees Celsius. Deposition is applied for multiple seconds.

In TEOS deposition step 316, the reactants including TEOS and molecular oxygen (O_2) are applied by a flow into the chamber 202 at a selected pressure and RF power. In an embodiment of the present invention using the NOVELLUS CONCEPT 1 (TM) PECVD reactor to fabricate wafers, the TEOS flow rate is approximately 1.8 ml/min, although flow rates from 1.6 ml/min to 2.0 ml/min are suitable. The oxygen (O_2) flow rate is approximately 6500 sccm, although flow rates from 6200 sccm to 6800 sccm are suitable. High frequency power applied at approximately 650 watts and low frequency power at approximately 350 watts although wattages that vary from these values by plus or minus five percent are also suitable. Pressure is applied at about 2.2 torr although pressures from 2.0

torr to 2.4 torr are suitable. The deposition temperature is about 400 degrees Celsius. Typically deposition is applied for approximately one minute, although exact timing is not critical.

The description of certain embodiments of this invention is intended to be illustrative and not limiting. Numerous other embodiments will be apparent to those skilled in the art, all of which are included within the broad scope of this invention. For example, A thin layer of silicon is grown by PECVD SiO_2 deposition using Silane (SiH_4) as the silicon source. In other embodiments of the fabrication method, other sources of silicon may be employed, including silicon tetrachloride ($SiCl_4$), trichlorosilane ($SiHCl_3$) or dichlorosilane (SiH_2Cl_2). Silane and dichorosilane are typically used for depositing relatively thin silicon epitaxial layers and for depositing epitaxial layers at a relatively low temperature.

What is claimed is:

CLAIMS:

1. A method of depositing a premetal interlayer dielectric on a semiconductor substrate using a PECVD reactor comprising the steps of:

depositing a plurality of layers of a premetal dielectric layer in in-situ deposition upon the semiconductor substrate the PECVD reactor with each subsequent layer being deposited after a previous layer with no intervening handling step;

cleaning the semiconductor substrate; and

chemical mechanical polishing the semiconductor substrate.

2. A method according to Claim 1 wherein the depositing step further includes substeps of:

depositing an undoped oxide layer;

depositing a phosphorus silicate glass layer; and

depositing a TEOS layer.

3. A method according to Claim 1 wherein the depositing step further includes substeps precedent to the undoped oxide layer depositing step, the phosphorus silicate glass layer depositing step and the TEO layer depositing step, the precedent substeps being the substeps of:

precoating an inner surface of the PECVD reactor; and

wafer temperature soaking the semiconductor substrate.

4. A premetal interlayer dielectric on a semiconductor substrate comprising:

an undoped liner/barrier layer coupled to the substrate;

a phosphorus silicate glass layer coupled to the undoped liner/barrier layer; and

an undoped TEO layer coupled to the phosphorus silicate glass layer.

5. A premetal interlayer dielectric on a semiconductor substrate wherein:

the undoped liner/barrier layer coupled to the substrate has a thickness of approximately 500 angstroms;

the phosphorus silicate glass layer coupled to the undoped liner/barrier layer has a thickness of approximately 3000 angstroms; and

the undoped TEO layer coupled to the phosphorus silicate glass layer has a thickness of approximately 10200 angstroms prior to polishing.

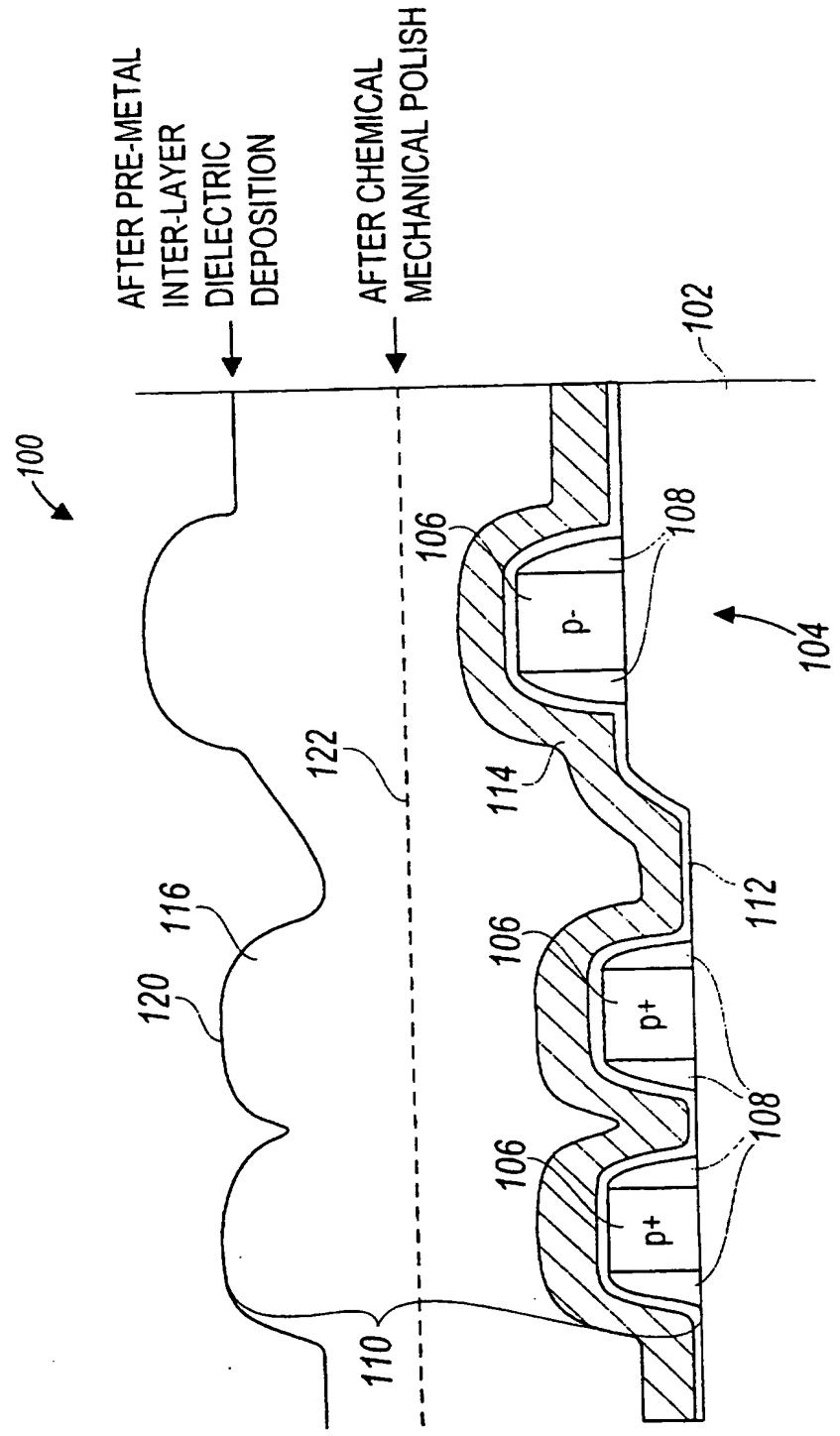
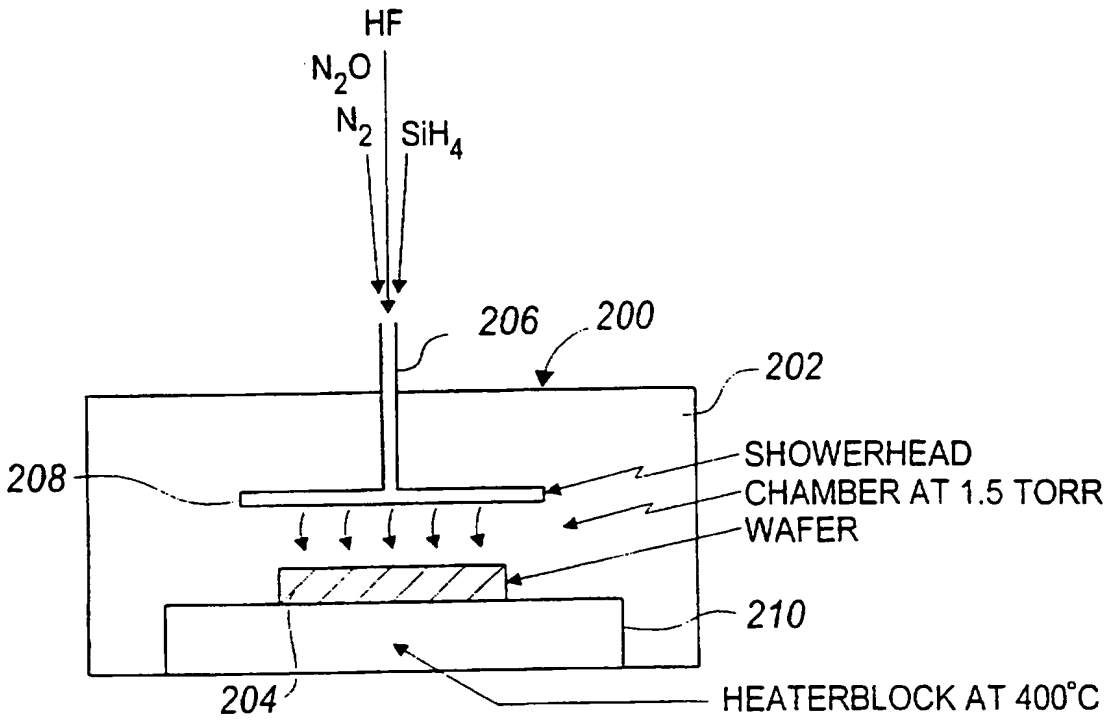


FIG. 1



- WAFER TEMPERATURE SOAK TIME = 18.5 SECS
- PRECOAT TIME (CHAMBER SEASONING) = 300 SECS

FIG. 2

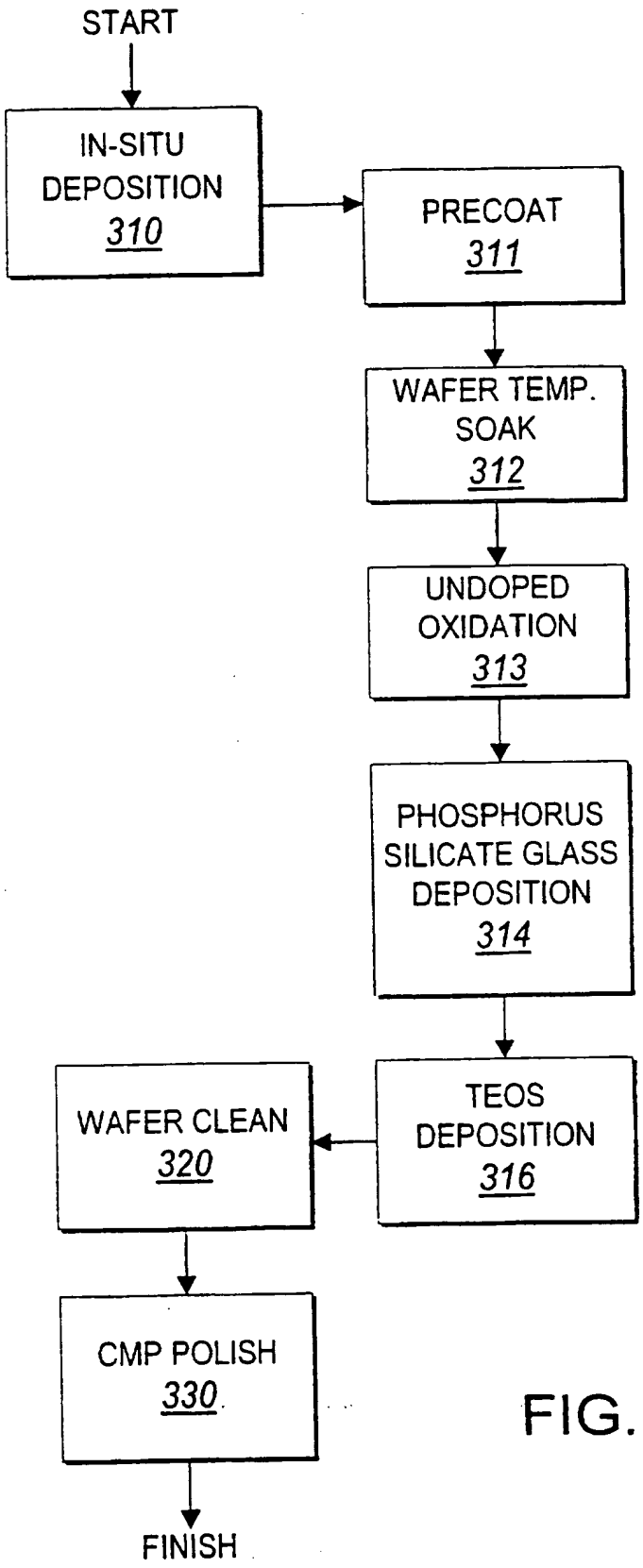


FIG. 3

INTERNATIONAL SEARCH REPORT

Inte .onal Application No
PCT/US 96/14340

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SPIE: MICROELECTRONICS TECHNOLOGY AND PROCESS INTEGRATION, 20 - 21 October 1994, AUSTIN,TEXAS,US, pages 2-11, XP002019336 M.K.JAIN ET AL.: "CHEMICAL MECHANICAL PLANARIZATION OF MULTILAYER DIELECTRIC STACKS" see page 2, paragraph 2 ---	1
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 266 (E-1551), 20 May 1994 & JP,A,06 045313 (NEC CORP), 18 February 1994, see abstract --- -/--	1

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 1996	09. 12. 96
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Authorized officer Schuermans, N

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte .onal Application No
PCT/US 96/14340

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 485 086 (AMERICAN TELEPHONE & TELEGRAPH) 13 May 1992 see column 2, line 32 - column 3, line 4 see column 4, line 15 - column 5, line 8 see column 7, line 3 - line 30 ---	2,4,5
A	RESEARCH DISCLOSURE, no. 325, 1 May 1991, page 367 XP000229723 "SI PRECOAT OF PECVD CHAMBER WALLS PRIOR TO THE FORMATION OF A THIN SI LAYER ON GAAS OR III-V COMPOUNDS" see page 367 -----	3

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte .onal Application No
PCT/US 96/14340

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0485086	13-05-92	JP-A- 4266028	22-09-92

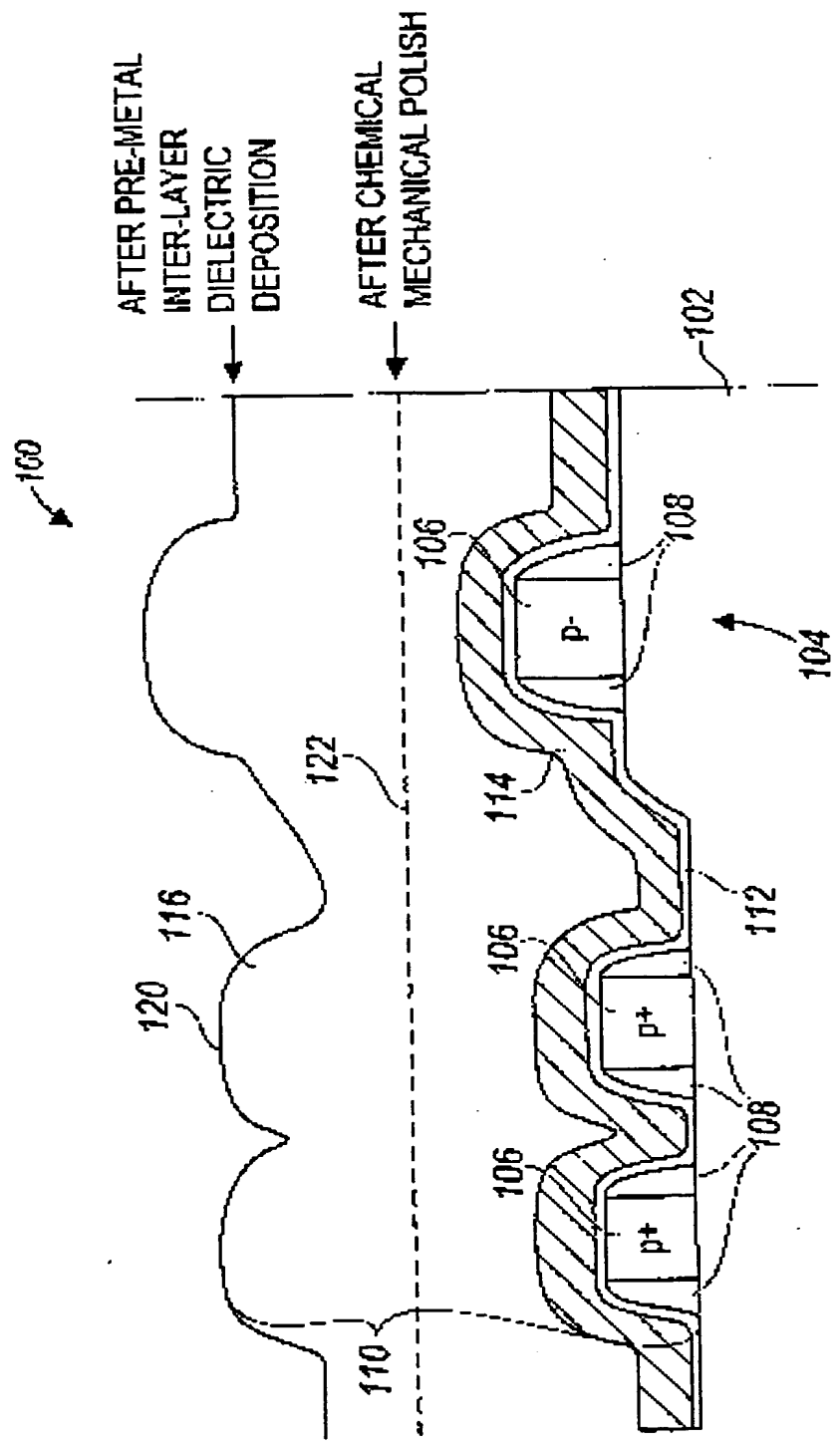
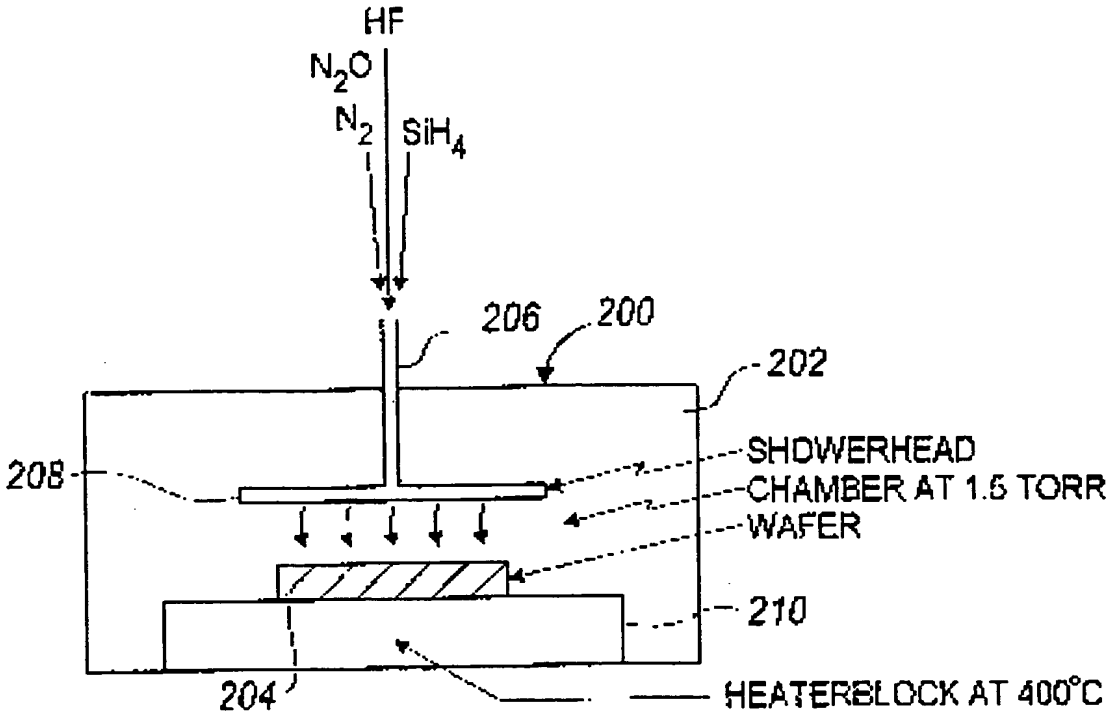


FIG. 1



- WAFER TEMPERATURE SOAK TIME = 18.5 SECS
- PRECOAT TIME (CHAMBER SEASONING) = 300 SECS

FIG. 2

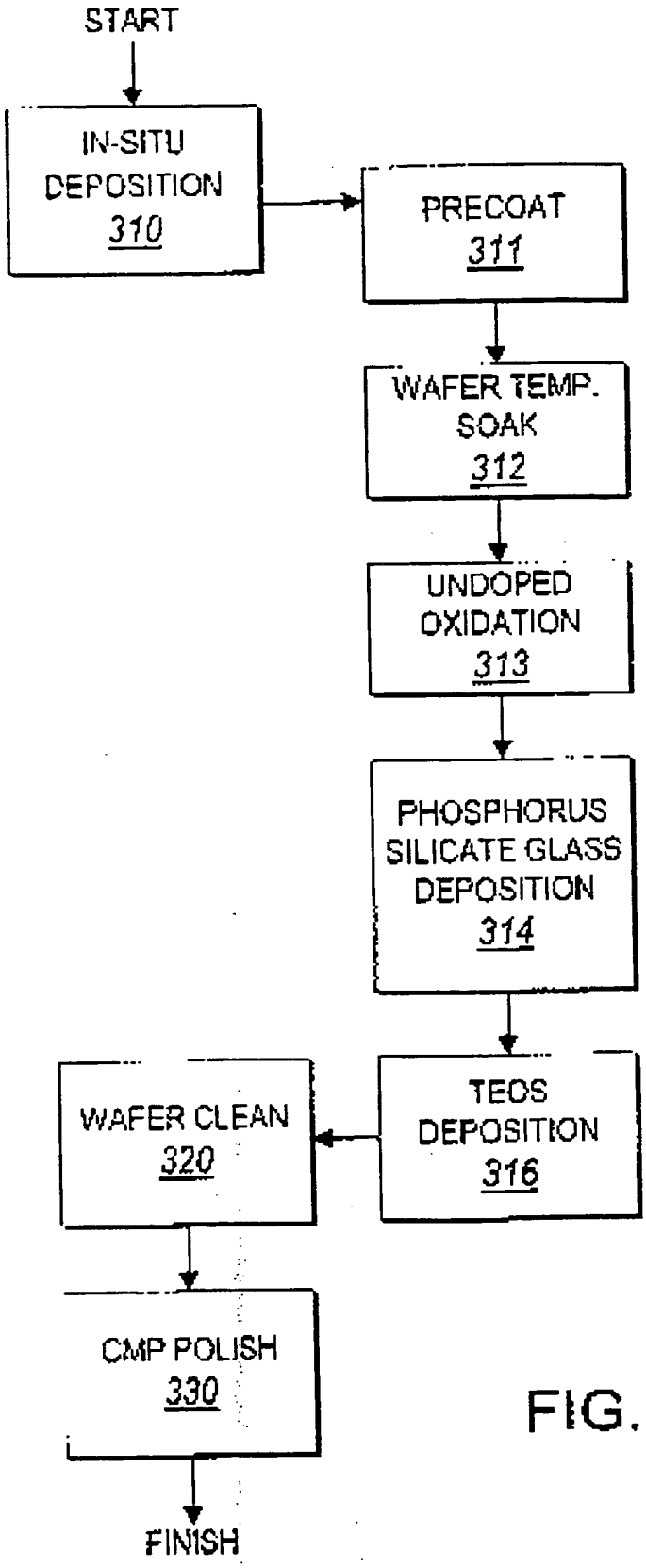


FIG. 3